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## Features

- Pulse-width Modulation up to 2 kHz Clock Frequency
- Protection Against Short-circuit, Load Dump Overvoltage and Reverse  $V_s$
- Duty Cycle 18% to 100% Continuously
- Internally Reduced Pulse Slope of Lamp's Voltage
- Interference and Damage Protection According to VDE 0839 and ISO/TR 7637/1
- Charge-pump Noise Suppression
- Ground-wire Breakage Protection

## 1. Description

The U6083B is a PWM IC in bipolar technology for the control of an N-channel power MOSFET used as a high-side switch. The IC is ideal for use in brightness control systems (dimming) of lamps, for example, in dashboard applications.



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## PWM Power Control IC with Interference Suppression

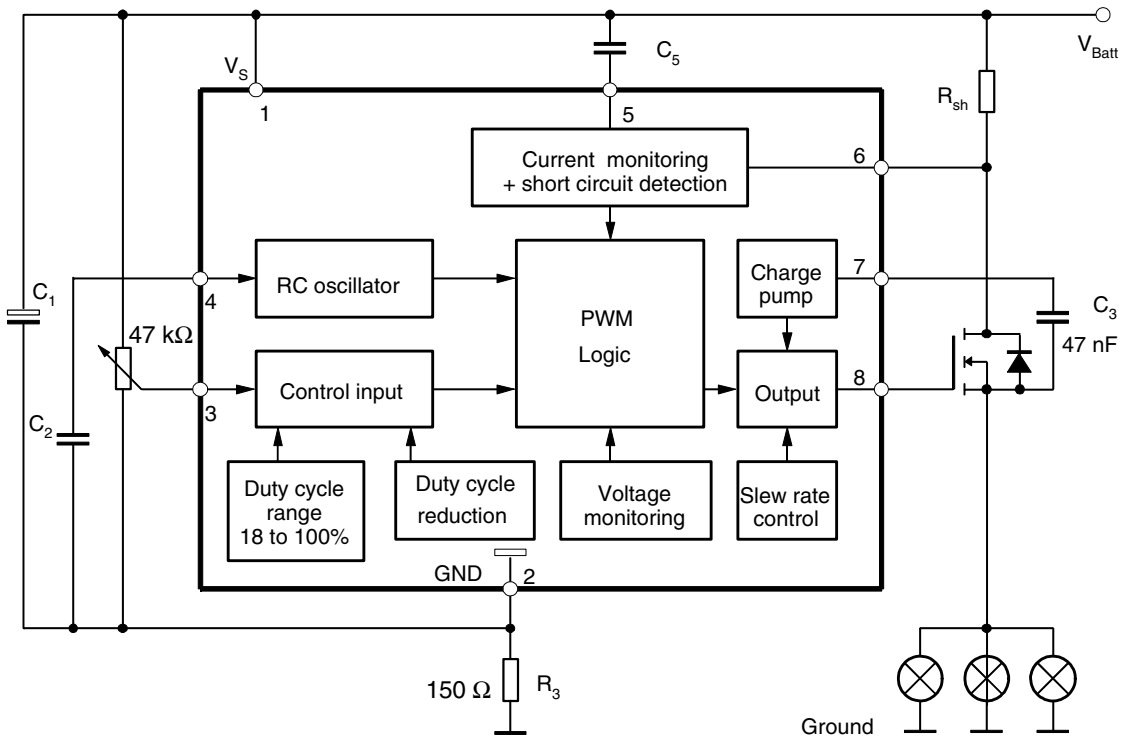
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### U6083B

Rev. 4770B-AUTO-09/05



**Figure 1-1.** Block Diagram with External Circuit



## 2. Pin Configuration

Figure 2-1. Pinning DIP8

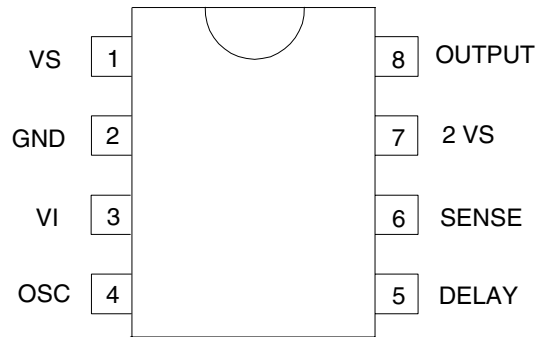


Table 2-1. Pin Description

Pin	Symbol	Function
1	VS	Supply voltage $V_S$
2	GND	IC ground
3	VI	Control input (duty cycle)
4	OSC	Oscillator
5	DELAY	Short-circuit protection delay
6	SENSE	Current sensing
7	2 VS	Voltage doubler
8	OUTPUT	Output

### 3. Functional Description

#### 3.1 Pin 1, Supply Voltage, $V_S$ or $V_{Batt}$

##### 3.1.1 Overvoltage Detection

###### 3.1.1.1 Stage 1

If overvoltages of  $V_{Batt} > 20V$  (typically) occur, the external transistor is switched off, and switched on again at  $V_{Batt} < 18.5V$  (hysteresis).

###### 3.1.1.2 Stage 2

If  $V_{Batt} > 28.5V$  (typically), the voltage limitation of the IC is reduced from  $V_S = 26V$  to  $20V$ . The gate of the external transistor remains at the potential of the IC ground, thus producing voltage sharing between FET and lamps in the event of overvoltage pulses (e.g., load dump). The short-circuit protection is not in operation. At  $V_{Batt}$  approximately  $< 23V$ , the overvoltage detection stage 2 is switched off. Thus, during overvoltage detection stage 2, the lamp voltage  $V_{lamp}$  is calculated as follows:

$$V_{Lamp} = V_{Batt} - V_S - V_{GS}$$

$V_S$  = supply voltage of the IC at overvoltage detection stage 2

$V_{GS}$  = gate - source voltage of the FET

##### 3.1.2 Undervoltage Detection

In the event of voltages of approximately  $V_{Batt} < 5.0V$ , the external FET is switched off and the latch for short-circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately  $V_{Batt} \geq 5.4V$ .

#### 3.2 Pin 2, GND

##### 3.2.1 Ground-wire Breakage

To protect the FET in the case of ground-wire breakage, a  $1\text{ M}\Omega$  resistor between gate and source is recommended to provide proper switch-off conditions.

#### 3.3 Pin 3, Control Input

The pulse width is controlled by means of an external potentiometer ( $47\text{ k}\Omega$ ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 18 to 100%. It is possible to further restrict the duty cycle with the resistors  $R_1$  and  $R_2$  (see [Figure 7-1 on page 11](#)).

In order to reduce the power dissipation of the FET and to increase the lifetime of the lamps, the IC automatically reduces the maximum duty cycle at pin 8 if the supply voltage exceeds  $V_2 = 13V$ . Pin 3 is protected against short-circuit to  $V_{Batt}$  and ground ( $V_{Batt} \leq 16.5V$ ).

### 3.4 Pin 4, Oscillator

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor,  $C_2$ . It is charged with a constant current,  $I$ , until the upper switching threshold is reached. A second current source is then activated which taps a double current,  $2 \times I$ , from the charging current. The capacitor,  $C_2$ , is thus discharged at the current,  $I$ , until the lower switching threshold is reached. The second source is then switched off again and the procedure starts once more.

#### 3.4.1 Example for Oscillator Frequency Calculation

Switching thresholds

$$V_{T100} = \text{High switching threshold (100\% duty cycle)}$$

$$V_{T100} = V_S \times \alpha_1 = (V_{\text{Batt}} - I_S \times R_3) \times \alpha_1$$

$$V_{T<100} = \text{High switching threshold (< 100\% duty cycle)}$$

$$V_{T<100} = V_S \times \alpha_2 = (V_{\text{Batt}} - I_S \times R_3) \times \alpha_2$$

$$V_{TL} = \text{Low switching threshold}$$

$$V_{TL} = V_S \times \alpha_3 = (V_{\text{Batt}} - I_S \times R_3) \times \alpha_3$$

where

$\alpha_1$ ,  $\alpha_2$  and  $\alpha_3$  are fixed values

#### 3.4.2 Calculation Example

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

$$V_{\text{Batt}} = 12\text{V}, I_S = 4 \text{ mA}, R_3 = 150\Omega, \alpha_1 = 0.7, \alpha_2 = 0.67 \text{ and } \alpha_3 = 0.28$$

$$V_{T100} = (12\text{V} - 4 \text{ mA} \times 150\Omega) \times 0.7 \approx 8\text{V}$$

$$V_{T<100} = 11.4\text{V} \times 0.67 = 7.6\text{V}$$

$$V_{TL} = 11.4\text{V} \times 0.28 = 3.2\text{V}$$

#### 3.4.3 Oscillator Frequency

3 cases have to be distinguished

1.  $f_1$  for duty cycle = 100%, no slope reduction with capacitor  $C_4$   
(see [Figure 7-1 on page 11](#))

$$f_1 = \frac{I_{\text{OSC}}}{2 \times (V_{T100} - V_{TL}) \times C_2}, \text{ where } C_2 = 68 \text{ nF}, I_{\text{OSC}} = 45 \mu\text{A}$$

$$f_1 = \dots = 75 \text{ Hz}$$

2.  $f_2$  for duty cycle < 100%, no slope reduction with capacitor  $C_4$

For a duty cycle of less than 100%, the oscillator frequency,  $f$ , is as follows:

$$f_2 = \frac{I_{\text{OSC}}}{2 \times (V_{T<100} - V_{TL}) \times C_2}, \text{ where } C_2 = 68 \text{ nF}, I_{\text{OSC}} = 45 \mu\text{A}$$

$$f_2 = \dots = 69 \text{ Hz}$$

3.  $f_3$  with duty cycle < 100% with slope reduction capacitor  $C_4$  (see “Output Slope Control” on page 6)

$$f_3 = \frac{I_{osc}}{2 \times (V_{T<100} - V_{TL}) \times C_2 + 2V_{Batt} \times C_4}$$

where  $C_2 = 68 \text{ nF}$ ,  $I_{OSC} = 45 \text{ }\mu\text{A}$ ,  $C_4 = 1.8 \text{ nF}$

$$f_3 = \dots = 70 \text{ Hz}$$

By selecting different values of  $C_2$  and  $C_4$ , it is possible to have a range of oscillator frequencies from 10 to 2000 Hz as shown in the data sheet.

### 3.5 Output Slope Control

The slope of the lamp voltage is internally limited to reduce radio interference by limitation of the voltage gain of the PWM comparator.

Thus, the voltage rise on the lamp is proportional to the oscillator voltage increase at the switchover time according to the equation.

$$dV_g/d_t = \alpha_4 \times dV_4/d_t = 2 \times \alpha_4 \times f \times (\alpha_2 - \alpha_3) \times (V_{Batt} - I_S \times R_3)$$

when

$$f = 75 \text{ Hz}, V_{TX} = V_T < 100 \text{ and } \alpha_4 = 63$$

then

$$dV_g/d_t = 2 \times 63 \times 75 \text{ Hz} \times (0.67 - 0.28) \times (12\text{V} - 4 \text{ mA} \times 15\Omega) = 42 \text{ V/ms}$$

Via an external capacitor,  $C_4$ , the slope can be further reduced as follows:

$$dV_g/d_t = I_{OSC}/(C_4 + C_2/\alpha_4)$$

when

$$I_{OSC} = 45 \text{ }\mu\text{A}, C_4 = 1.8 \text{ nF}, C_2 = 68 \text{ nF and } \alpha_4 = 63$$

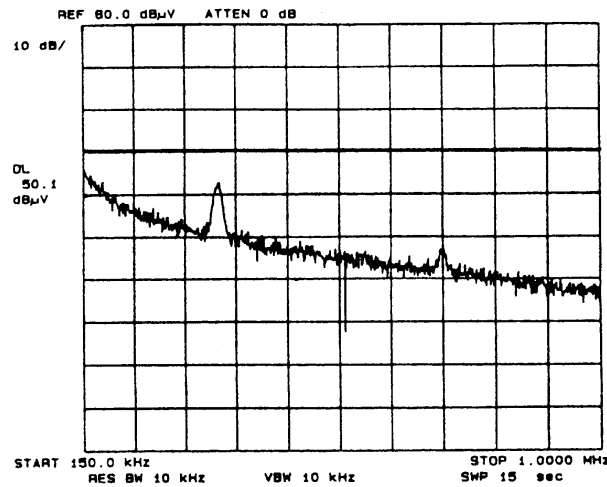
$$\text{then } dV_g/d_t = 45 \text{ }\mu\text{A}/(1.8 \text{ nF} + 68 \text{ nF}/63) = 15.6 \text{ V/ms}$$

To damp oscillation tendencies, a resistance of  $100\Omega$  in series with capacitance  $C_4$  is recommended.

### 3.6 Interference Suppression

- “On-board” radio reception according to VDE 0879 part 3/4.81
- Test conditions referring to [Figure 3-1](#)
- Application circuit according to [Figure 1-1 on page 2](#) or [Figure 7-1 on page 11](#)
- Load: nine 4W lamps in parallel
- Duty cycle = 18%
- $V_{Batt} = 12V$
- $f_{Osc} = 100\text{ Hz}$

**Figure 3-1.** Voltage Spectrum of On-board Radio Reception



### 3.7 Pins 5 and Pin 6, Short-circuit Protection and Current Sensing

#### 3.7.1 Short-circuit Detection and Time Delay, $t_d$

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ( $V_{T2} \approx 90\text{ mV}$ ), the duty cycle is switched over to 100% and the capacitor  $C_5$  is charged by a current source of  $I_{ch} - I_{dis}$ . The external FET again is switched off after the cut-off threshold ( $V_{T5}$ ) is reached. Switching on the FET again is possible after a power-on reset only. The current source,  $I_{dis}$ , ensures that the capacitor  $C_5$  is not charged by parasitic currents.

The time delay,  $t_d$ , is calculated as follows:

$$t_d = C_5 \times V_{T5} / (I_{ch} - I_{dis})$$

With  $C_5 = 100\text{ nF}$  and  $V_{T5} = 10.4V$ ,  $I_{ch} = 13\text{ }\mu A$ ,  $I_{dis} = 3\text{ }\mu A$ , the time delay is as follows:

$$t_d = 100\text{ nF} \times 10.4V / (13\text{ }\mu A - 3\text{ }\mu A)$$

$$t_d = 104\text{ ms}$$

### 3.7.2 Current Limitation

The lamp current is limited by a control amplifier to protect the external power transistor. The voltage drop across the external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of  $V_{T1} \approx 100$  mV. Owing to the difference  $V_{T1} - V_{T2} \approx 10$  mV, it ensures that current limitation occurs only when the short-circuit detection circuit has responded.

After a power-on reset, the output is inactive for half an oscillator cycle. During this time, the supply voltage capacitor can be charged so that current limitation is guaranteed in the event of a short-circuit when the IC is switched on for the first time.

### 3.8 Pins 7 and 8, Charge Pump and Output

Pin 8 (output) is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor  $C_3$  (bootstrapping). In addition, a trickle charge is generated by an integrated oscillator ( $f_7 \approx 400$  kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.



## 4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Junction temperature	$T_j$	150	°C
Ambient temperature range	$T_{amb}$	-40 to +110	°C
Storage temperature range	$T_{stg}$	-55 to +125	°C

## 5. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	$R_{thJA}$	120	K/W

## 6. Electrical Characteristics

$T_{amb} = -40^{\circ}\text{C}$  to  $+110^{\circ}\text{C}$ ,  $V_{Batt} = 9\text{V}$  to  $16.5\text{V}$ , (basic function is guaranteed between  $6.0\text{V}$  to  $9.0\text{V}$ ) reference point ground, unless otherwise specified (see [Figure 1-1 on page 2](#)). All other values refer to pin GND (pin 2).

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Current consumption		1	$I_S$			7.9	mA
Supply voltage	Oversvoltage detection, stage 1		$V_{Batt}$			25	V
Stabilized voltage	$I_S = 10\text{ mA}$	1	$V_S$	24.5		27.0	V
Battery undervoltage detection	on		$V_{Batt}$	4.4	5.0	5.6	V
	off			4.8	5.4	6.0	
<b>Battery Oversvoltage Detection</b>							
Stage 1:	on		$V_{Batt}$	18.3	20.0	21.7	V
	off			16.7	18.5	20.3	
Stage 2: Detection stage 2	on		$V_{Batt}$	25.5	28.5	32.5	V
	off			19.5	23.0	26.5	
Stabilized voltage	$I_S = 30\text{ mA}$	1	$V_S$	18.5	20.0	21.5	V
<b>Short-circuit Protection</b>		6					
Short-circuit current limitation	$V_{T1} = V_S - V_6$		$V_{T1}$	85	100	120	mV
Short-circuit detection	$V_{T2} = V_S - V_6$		$V_{T2}$	75	90	105	mV
	$V_{T2} = V_S - V_6$		$V_{T1} - V_{T2}$	3	10	30	mV
<b>Delay Timer Short-circuit Detection, <math>V_{Batt} = 12\text{V}</math></b>		5					
Switched off threshold	$V_{T5} = V_S - V_5$		$V_{T5}$	10.2	10.4	10.6	V
Charge current			$I_{ch}$		13		$\mu\text{A}$
Discharge current			$I_{dis}$		3		$\mu\text{A}$
Capacitance current	$I_5 = I_{ch} - I_{dis}$		$I_5$	5	10	15	mA

Note: 1. Reference point is battery ground

## 6. Electrical Characteristics (Continued)

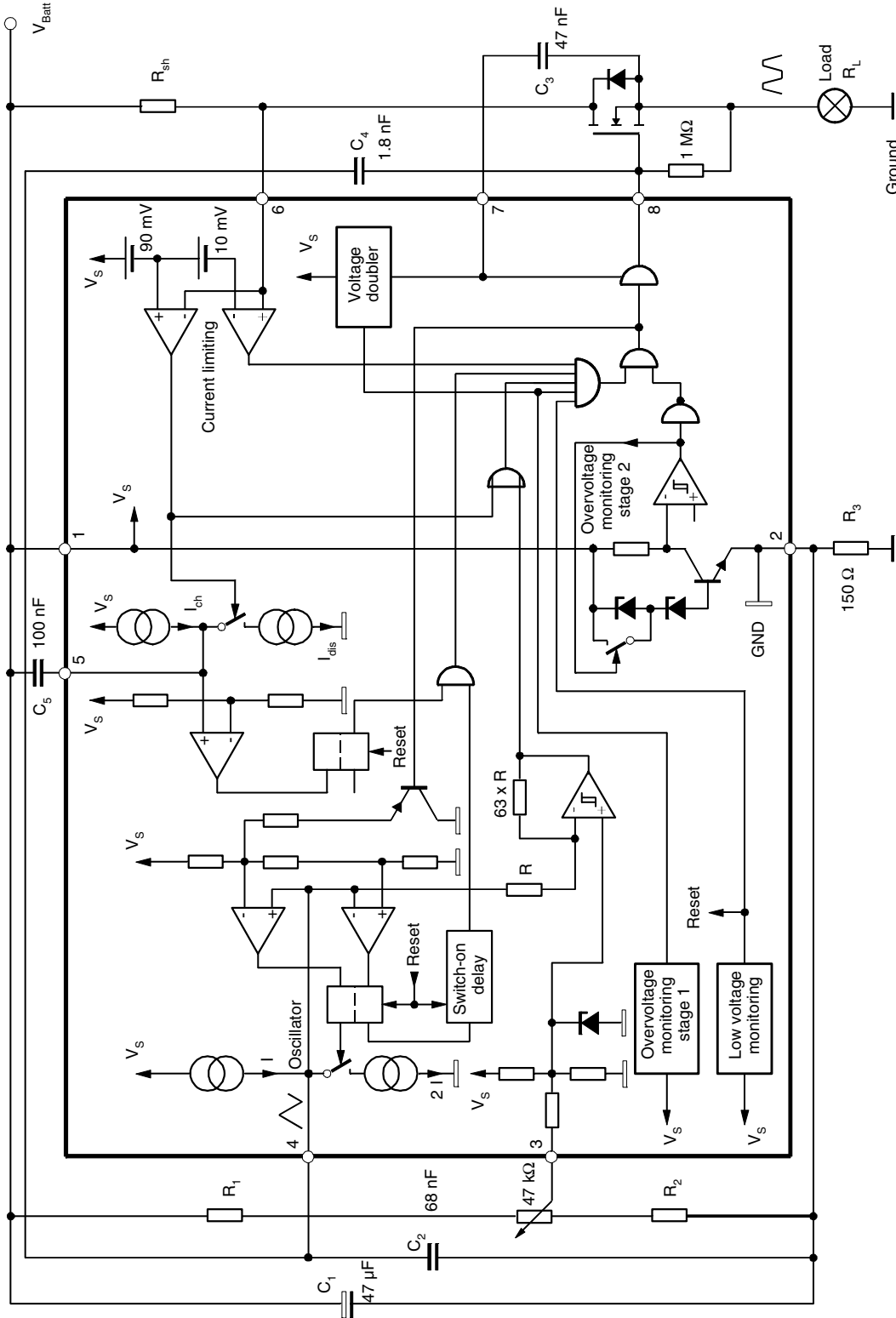
$T_{amb} = -40^{\circ}\text{C}$  to  $+110^{\circ}\text{C}$ ,  $V_{Batt} = 9\text{V}$  to  $16.5\text{V}$ , (basic function is guaranteed between  $6.0\text{V}$  to  $9.0\text{V}$ ) reference point ground, unless otherwise specified (see Figure 1-1 on page 2). All other values refer to pin GND (pin 2).

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
<b>Voltage Doubler</b>		7					
Voltage	Duty cycle 100%		$V_7$	$2 V_S$			
Oscillator frequency			$f_7$	280	400	520	kHz
Internal voltage limitation	$I_7 = 5\text{ mA}$ (whichever is lower)		$V_7$	26	27.5	30.0	V
			$V_7$	$V_{S+14}$	$V_{S+15}$	$V_{S+16}$	V
Edge steepness	$dv_g/dt = \alpha_4 dv_4/dt$ $dV_g/dt_{max}$		$\alpha_4$	53	63	72 130	V/ms
<b>Gate Output</b>		8					
Voltage	Low level		$V_8$	0.35	0.70	0.95	V
	$V_{Batt} = 16.5\text{V}$ $T_{amb} = 110^{\circ}\text{C}$ , $R_3 = 150\Omega$		$V_8$			1.5 <sup>(1)</sup>	V
	High level, duty cycle 100%		$V_8$		$V_7$		V
Current	$V_8 = \text{Low level}$		$I_8$	1.0			mA
	$V_8 = \text{High level, } I_7 >  I_8 $		$I_8$	-1.0			mA
Duty cycle	Min: $C_2 = 68\text{ nF}$		$t_p/T$	15	18	21	%
	Max: $V_{Batt} \leq 12.4\text{V}$			100			
	$V_{Batt} = 16.5\text{V}$ , $C_2 = 68\text{ nF}$			65	73	81	
<b>Oscillator</b>							
Frequency		4	f	10		2000	Hz
Threshold cycle	$V_8 = \text{High, } \alpha_1 = \frac{V_{T100}}{V_S}$		$\alpha_1$	0.68	0.7	0.72	
Upper	$V_8 = \text{Low, } \alpha_2 = \frac{V_{T<100}}{V_S}$		$\alpha_2$	0.65	0.67	0.69	
Lower	$\alpha_3 = \frac{V_{TL}}{V_S}$		$\alpha_3$	0.26	0.28	0.3	
Oscillator current	$V_{Batt} = 12\text{V}$		$\pm I_{OSC}$	34	45	54	$\mu\text{A}$
Frequency	$C_4$ open, $C_2 = 68\text{ nF}$ duty cycle = 50%		f	56	75	90	Hz

Note: 1. Reference point is battery ground

## 7. Application

Figure 7-1. Application Circuit



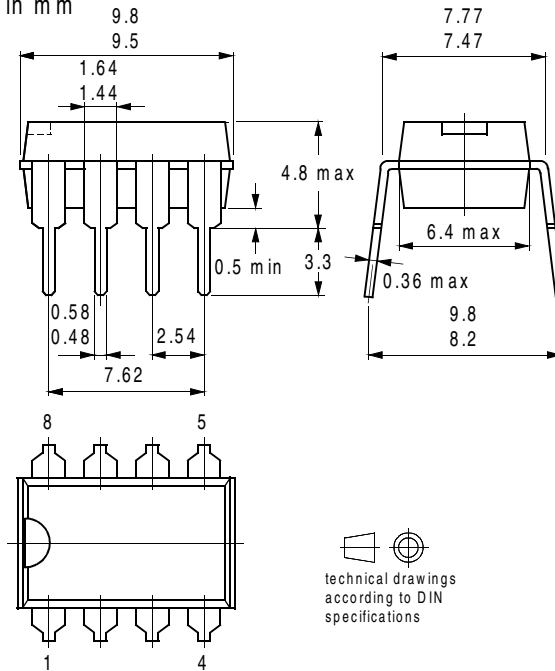
## 8. Ordering Information

Extended Type Number	Package	Remarks
U6083B-MY	DIP8	Pb-free

## 9. Package Information

### Package DIP8

Dimensions in mm





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